5600 User's Manual

Doc. #02796 Rev 0393

OCTAGON SYSTEMS CORPORATION®

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IMPORTANT!

Please read before installing your product.

Octagon's products are designed to be high in performance while consuming very little power. In order to maintain this advantage, CMOS circuitry is used.

CMOS chips have specific needs and some special requirements that the user must be aware of. Read the following to help avoid damage to your card from the use of CMOS chips.

Using CMOS Circuitry in Industrial Control

Industrial computers originally used LSTTL circuits. Because many PC components are used in laptop computers, IC manufacturers are exclusively using CMOS technology. Both TTL and CMOS have failure mechanisms, but they are different. This section describes some of the common failures which are common to all manufacturers of CMOS equipment. However, much of the information has been put in the context of the Micro PC.

Octagon has developed a reliable database of customer-induced, field failures. The average MTBF of Micro PC cards exceeds 11 years, yet there are failures. Most failures have been identified as customer-induced, but there is a small percentage that cannot be identified. As expected, virtually all the failures occur when bringing up the first system. On subsequent systems, the failure rate drops dramatically.

- Approximately 20% of the returned cards are problem-free. These cards, typically, have the wrong jumper settings or the customer has problems with the software. This causes frustration for the customer and incurs a testing charge from Octagon.

- Of the remaining 80% of the cards, 90% of these cards fail due to customer misuse and accident. Customers often cannot pinpoint the cause of the misuse.

- Therefore, 72% of the returned cards are damaged through some type of misuse. Of the remaining 8%, Octagon is unable to determine the cause of the failure and repairs these cards at no charge if they are under warranty.

The most common failures on CPU cards are over voltage of the power supply, static discharge, and damage to the serial and parallel ports. On expansion cards, the most common failures are static discharge, over voltage of inputs, over current of outputs, and misuse of the CMOS circuitry with regards to power supply sequencing. In the case of the video cards, the most common failure is to miswire the card to the flat panel display. Miswiring can damage both the card and an expensive display.

- **Multiple component failures** - The chance of a random component failure is very rare since the average MTBF of an Octagon card is greater than 11 years. In a 7 year study,

Octagon has never found a single case where multiple IC failures were not caused by misuse or accident. It is very probable that multiple component failures indicate that they were user-induced.

- **Testing "dead" cards** - For a card that is "completely nonfunctional", there is a simple test to determine accidental over voltage, reverse voltage or other "forced" current situations. Unplug the card from the bus and remove all cables. Using an ordinary digital ohmmeter on the 2,000 ohm scale, measure the resistance between power and ground. Record this number. Reverse the ohmmeter leads and measure the resistance again. If the ratio of the resistances is 2:1 or greater, fault conditions most likely have occurred. A common cause is miswiring the power supply.

- **Improper power causes catastrophic failure** - If a card has had reverse polarity or high voltage applied, replacing a failed component is not an adequate fix. Other components probably have been partially damaged or a failure mechanism has been induced. Therefore, a failure will probably occur in the future. For such cards, Octagon highly recommends that these cards be replaced.

- **Other over-voltage symptoms** - In over-voltage situations, the programmable logic devices, EPROMs and CPU chips, usually fail in this order. The failed device may be hot to the touch. It is usually the case that only one IC will be overheated at a time.

- **Power sequencing** - The major failure of I/O chips is caused by the external application of input voltage while the Micro PC power is off. If you apply 5V to the input of a TTL chip with the power off, nothing will happen. Applying a 5V input to a CMOS card will cause the current to flow through the input and out the 5V power pin. This current attempts to power up the card. Most inputs are rated at 25 mA maximum. When this is exceeded, the chip may be damaged.

- **Failure on power-up** - Even when there is not enough current to destroy an input described above, the chip may be destroyed when the power to the card is applied. This is due to the fact that the input current biases the IC so that it acts as a forward biased diode on power-up. This type of failure is typical on serial interface chips.

- **Serial and parallel** - Customers sometimes connect the serial and printer devices to the Micro PC while the power is off. This can cause the failure mentioned in the above section, *Failure upon power-up*. Even if they are connected with the Micro PC on, there can be another failure mechanism. Some serial and printer devices do not share the same power (AC) grounding. The leakage can cause the serial or parallel signals to be 20-40V above the Micro PC ground, thus, damaging the ports as they are plugged in. This would not be a problem if the ground pin is connected first, but there is no guarantee of this. Damage to the printer port chip will cause the serial ports to fail as they share the same chip.

- **Hot insertion** - Plugging cards into the card cage with the power on will usually not cause a problem. (**Octagon urges that you do not do this!**) However, the card may be damaged if the right sequence of pins contacts as the card is pushed into the socket. This usually damages bus driver chips and they may become hot when the power is applied. This is one of the most common failures of expansion cards.

- **Using desktop PC power supplies** - Occasionally, a customer will use a regular desktop PC power supply when bringing up a system. Most of these are rated at 5V at 20A or more. Switching supplies usually require a 20% load to operate properly. This means 4A or more. Since a typical Micro PC system takes less than 2A, the supply does not regulate properly. Customers have reported that the output can drift up to 7V and/or with 7-8V voltage spikes. Unless a scope is connected, you may not see these transients.

- **Terminated backplanes** - Some customers try to use Micro PC cards in backplanes that have resistor/capacitor termination networks. CMOS cards cannot be used with termination networks. Generally, the cards will function erratically or the bus drivers may fail due to excessive output currents.

- **Excessive signal lead lengths** - Another source of failure that was identified years ago at Octagon was excessive lead lengths on digital inputs. Long leads act as an antenna to pick up noise. They can also act as unterminated transmission lines. When 5V is switch onto a line, it creates a transient waveform. Octagon has seen submicrosecond pulses of 8V or more. The solution is to place a capacitor, for example 0.1 µF, across the switch contact. This will also eliminate radio frequency and other high frequency pickup.

NOTICE

The 5600-48 is a 48 line version of the 5600 Digital I/O Card. Jumpers J3 and J4 and corresponding 82C55 ICs at U3 and U4 have been removed. When using the 5600-48, refer to the User's Manual for information on connectors J1 and J2.

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WARRANTY

PREFACE

This manual is a guide to the proper configuration and operation of your 5600 Digital I/O Card. Installation instructions, card mapping information and jumpering options are described in the main body of the manual; technical specifications are included in the appendices.

The 5600 is a 96–channel digital I/O card designed to be used with any Octagon Micro PC Control Card. This combination provides a modular system which is easy to set up, modify and use. You can also use your 5600 in conjunction with other Micro PC expansion cards, allowing you to tailor your system for a wide variety of applications.

All Micro PC products are modular, so creating a system is as easy as selecting and plugging in the products you need.

CONVENTIONS USED IN THIS MANUAL

1. Information which appears on your screen (output from your system or commands or data that you key in) is shown in a different type face.

   Example 1:

   ```
   Octagon 5600 ROM BIOS Vers X.XX
   Copyright (c) 1990, Octagon Systems, Corp.
   All rights reserved
   ```

   Example 2:

   Press the <ESC> key.

2. Italicized refers to information that is specific to your particular system or program, for example,

   Enter *filename*

   means enter the name of your file. Names of other sections or manuals are also italicized.

3. Warnings always appear in this format:

   WARNING: The warning message appears here.

4. Paired angle brackets are used to indicate a specific key on your keyboard, for example, <ESC> means the escape key; <CTRL> means the control key; <F1> means the F1 function key.

5. All addresses are given in hexadecimal.

SYMBOLS AND TERMINOLOGY

Throughout this manual, the following symbols and terminology are used:

W[–]	Denotes a jumper block and the pins to connect.
NOTE	Information under this heading presents helpful tips for using the 5600.
WARNING:	Information under this heading warns you of situations which might cause catastrophic or irreversible damage.
PC SmartLINK	A serial communications software package designed by Octagon. It provides communications between a PC and other equipment and may be used with any PC software package, including CAMBASIC IV. Refers to all versions of PC SmartLINK.
Reset	Resetting the system hardware and software by pushing the reset switch. Has the same results as disconnecting power to the system, without the potential side effects of a cold reset.
TTL Compatible	0–5V logic levels.
H	The suffix "H" denotes a hexadecimal number. For example, 1000H in hexadecimal equals 4096 in decimal.

TECHNICAL SUPPORT

If you have a question about the 5600 Digital I/O Card and can't find the answer in this manual, call our Technical Support Department. They will be ready to give you the assistance you need.

When you call, please have the following at hand:

Your *5600 Digital I/O Card User's Manual*

A description of your problem

The direct line to the Technical Support Department is 303–426–4521

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DESCRIPTION

The 5600 is a general purpose digital I/O card designed for use with the Octagon Micro PC system. It accepts switch closures and logic inputs, drives displays and LEDs, and interfaces with opto module racks. The 5600 will interface with most types of digital I/O, including LCD (liquid crystal display) series and DP (vacuum fluorescent) series displays, printers, keyboards, and single LEDs. See *Figure 1–1* for a typical system configuration using the 5600.

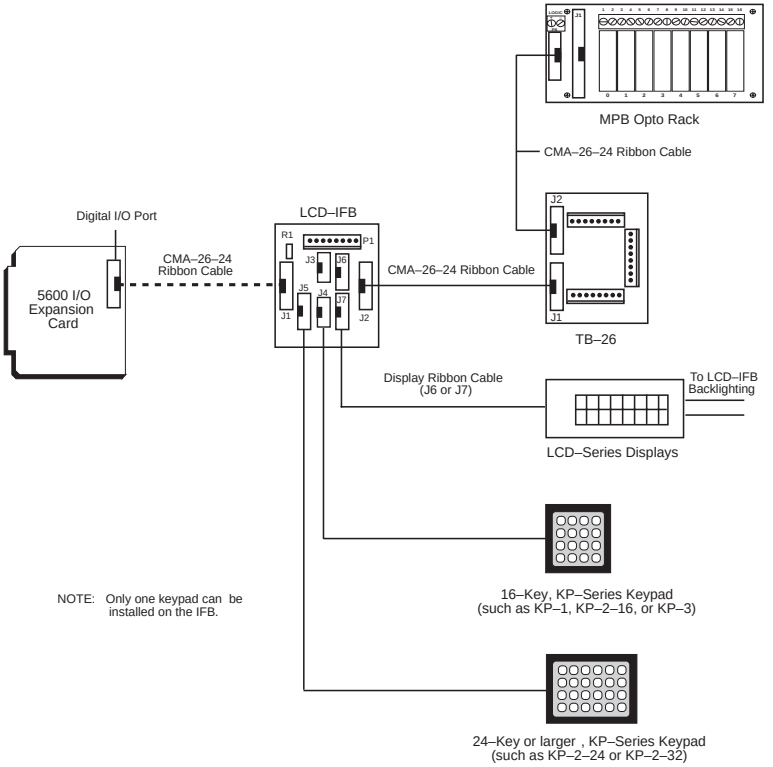
MPB Opto Rack
CMA–26–24 Ribbon Cable
Digital I/O Port
LCD–IFB
CMA–26–24 Ribbon Cable
5600 I/O Expansion Card
CMA–26–24 Ribbon Cable
TB–26
Display Ribbon Cable (J6 or J7)
To LCD–IFB Backlighting
LCD–Series Displays
NOTE: Only one keypad can be installed on the IFB.
16–Key, KP–Series Keypad (such as KP–1, KP–2–16, or KP–3)
24–Key or larger , KP–Series Keypad (such as KP–2–24 or KP–2–32)

Figure 1–1—Typical 5600 system configuration

The card measures 4.5 x 4.9 inches and uses one slot of the Micro PC card cage. It is compatible with all Micro PC Control Cards and is electrically compatible with standard–sized CPU cards. It requires 5 volts at 35 mA typical.

The 5600 has 96 lines which are grouped into 12 ports of 8 lines each. Using software, you may configure channels as inputs or outputs in groups of 4 or 8 lines. All 96 lines may be nonlatched inputs or latched outputs. Up to 64 lines may be latched inputs. Each I/O line has a 10K pullup resistor; external resistors are not required when using switch contacts.

All 96 I/O lines are TTL compatible. A low level input signal is defined from –0.3V to 0.8V and a high level input signal is 2.0V to 5.0V. A low level output is 0.0V to 0.4V and a high level output is 2.4V to 5.0V.

The 5600 is based on the Intel 82C55A programmable input/output chip. Four of these are used in each 5600 to provide the 96 I/O lines. For detailed information on the 82C55A and its additional features, please refer to the Intel documentation included in Appendix B and the Intel Peripherals databook.

Chapter 2 INSTALLATION

The 5600 Digital I/O Card uses one slot of the Micro PC card cage. It may be used with any Micro PC Control Card.

WARNING: The 5600 contains static sensitive CMOS components. The greatest danger occurs when the card is plugged into a card cage. The 5600 becomes charged by the user and the static discharges to the backplane from the pin closest to the card connector. If that pin happens to be an input pin, even TTL inputs may be damaged. To avoid damaging your card and its components:

1. Ground yourself before handling the 5600 Digital I/O Card.
2. Disconnect power before removing or inserting the 5600 Card.

EQUIPMENT

You will need the following equipment (or equivalent) to use your 5600.

- 5600 Digital I/O Card
- Micro PC Card Cage
- Power Supply or Module
- PC SmartLINK or other communications software.

INSTALLATION

Before installing the 5600 Digital I/O Card, refer to Figure 2–1 for the location of various connectors and jumpers.

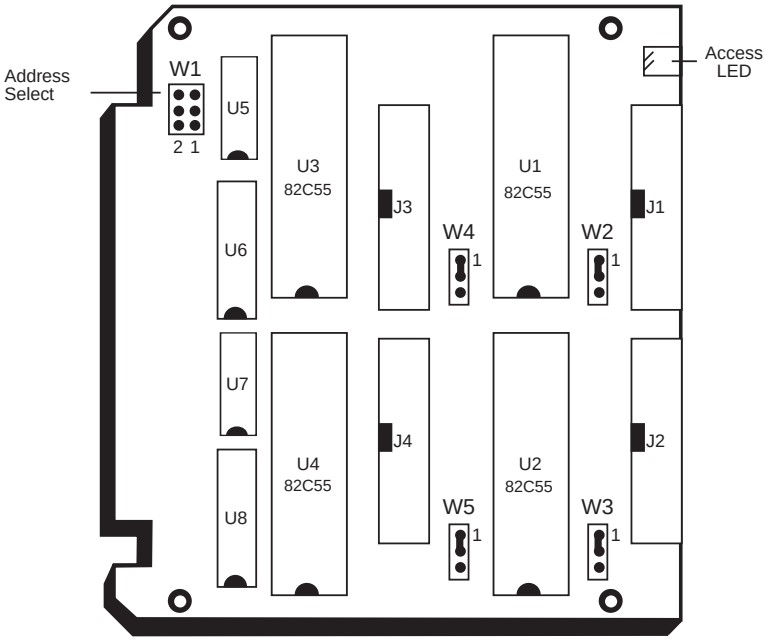

Figure 2–1—5600 Component Diagram

Base Address

The 5600 is configured at the factory to operate in most systems without any jumper changes. Jumper block W1 defines the base address. As shipped, the base address is 100H, which is jumper configuration W1[1–2, 3–4, 5–6]. If there is another card in your system with a base address of 100H, you must use a different base address for the 5600 or the other expansion card.

To change the base address, change the jumper connections in block W1. Connect the appropriate pins with push–on connectors. *Table 2–1* lists the jumper connections and corresponding base addresses.

Base Address Select: W1	
Pins Jumpered	**Base Address**
[1-2][3-4][5-6]	100H*
[3-4][5-6]	110H
[1-2][5-6]	120H
[5-6]	130H
[1-2][3-4]	140H
[3-4]	150H
[1-2]	160H
Not jumpered	170H

* = default

To install the 5600 in the card cage:

WARNING: Take care to correctly position the 5600 in the card cage. The V_{CC} and ground signals must match those on the backplane. Figure 2–2 shows the relative position of the 5600 as it is installed in the card cage.

1. Verify the base address settings are correct for your appli–cation.

2. Turn card cage power off.

3. Position the cage so that the backplane is away from you, the power module is to the right, and the open side of the cage is closest to you. The lettering on the backplane should be right side up (for example, you should be able to read “A31” on the backplane), with the words “OCTAGON SYSTEMS CORP.” running vertically along the left side of the backplane. This position is “feet down” for a table mount cage and “feet back” for a rear mount.

4. Slide the 5600 into the card cage. The components on the card should face to the left. The lettering on the card ("Octagon Systems Corp.") should be on the top edge of the card and the gold contact fingers toward the backplane.

5. Plug the 5600 into the backplane.

6. The amber LED will light briefly whenever the card is accessed (input or output).

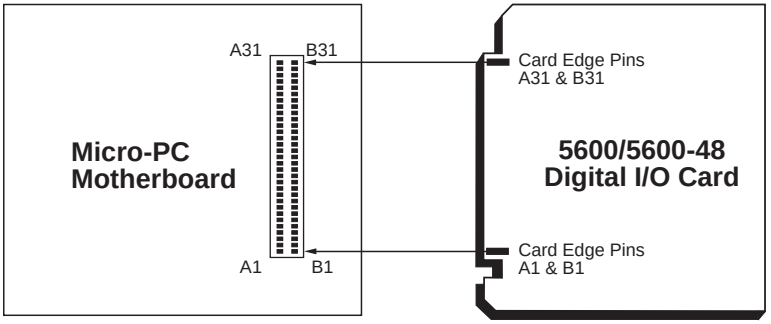

Figure 2–2—Card Edge Orientation

PORT PINOUTS

The pinouts are identical for each connector (J1 through J4). Each connector has 24 I/O lines (3 ports), 5 volts and ground. The individual ports are designated A, B, and C. Port A has the lowest address; each half of port C is controllable (upper and lower C). Each port pin has a 10K pull–up resistor. *Table 2–2* shows the connector pinouts for each port.

Digital I/O: J1-J4	
Pin #	**Function**
19	Port A, line 0
21	Port A, line 1
23	Port A, line 2
25	Port A, line 3
24	Port A, line 4
22	Port A, line 5
20	Port A, line 6
18	Port A, line 7
10	Port B, line 0
8	Port B, line 1
4	Port B, line 2
6	Port B, line 3
1	Port B, line 4
3	Port B, line 5
5	Port B, line 6
7	Port B, line 7
13	Port C, line 0
16	Port C, line 1
15	Port C, line 2
17	Port C, line 3
14	Port C, line 4
11	Port C, line 5
12	Port C, line 6
9	Port C, line 7
2	+5V
26	Common

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PORT ADDRESSES

The 5600 uses a block of 16 addresses. Within the block are four groups of four addresses. The first three in each group access 8–bit ports; the fourth address is the control register for that group. The following table shows the addresses of the ports in the 16 address blocks.

Port Address Functions	
Function	**Port Address**
J1, Port A	Base + 00H
J1, Port B	Base + 01H
J1, Port C	Base + 02H
J1, Control Register	Base + 03H
J2, Port A	Base + 04H
J2, Port B	Base + 05H
J2, Port C	Base + 06H
J2, Control Register	Base + 07H
J3, Port A	Base + 08H
J3, Port B	Base + 09H
J3, Port C	Base + 0AH
J3, Control Register	Base + 0BH
J4, Port A	Base + 0CH
J4, Port B	Base + 0DH
J4, Port C	Base + 0EH
J4, Control Register	Base + 0FH

For a complete description of the capabilities of the 82C55A, please refer to the information in Appendix B and to the Intel Peripheral Databook. Some of the chip's capabilities are described below.

On power–up or reset, all three ports are in the input state. You can alter which ports are inputs or outputs by writing a control command to the control register in the 82C55A. The examples below assume the base address is 100H.

For example, if you want all three ports to be outputs, use

```
OUT &H103,&H80
```

Port A will now output all “1”s after:

```
OUT &H100,&HFF
```

or all “0”s after:

```
OUT &H100,0
```

82C55 Control Register Commands					
HEX	**DEC**	**Port A***	**Port B***	**Port UC***	**Port LC***
80H	128	OUT	OUT	OUT	OUT
81H	129	OUT	OUT	OUT	IN
82H	130	OUT	IN	OUT	OUT
83H	131	OUT	IN	OUT	IN
88H	136	OUT	OUT	IN	OUT
89H	137	OUT	OUT	IN	IN
8AH	138	OUT	IN	IN	OUT
8BH	139	OUT	IN	IN	IN
90H	144	IN	OUT	OUT	OUT
91H	145	IN	OUT	OUT	IN
92H	146	IN	IN	OUT	OUT
93H	147	IN	IN	OUT	IN
98H	152	IN	OUT	IN	OUT
99H	153	IN	OUT	IN	IN
9AH	154	IN	IN	IN	OUT
9BH	155	IN	IN	IN	IN

* Ports A and B must be either all inputs of all outputs. Each half of Port C is controllable. Upper C (UC) includes bits 4 through 7 and Lower C (LC) includes bits 0 through 3.

Example

The statement,

```
OUT &H103,&H99
```

will turn A and C into 8–bit input ports and port B into an 8–bit output port (assuming the base address is 100H).

These examples describe only one of three possible modes of operation (Mode 0) as described in the 82C55 data sheet in Appendix B.

PULLING THE I/O LINES HIGH OR LOW

Jumper blocks W2–W5 pull all of the 24 I/O lines of the corresponding connector high or low. The factory default sets all of the I/O lines high.

Configuring I/O Lines: W2-W5			
Jumper Block	**Pins Jumpered**	**Description**	**Connector**
W2	[1-2]* [2-3]	+5 GND	J1
W3	[1-2]* [2-3]	+5 GND	J2
W4	[1-2]* [2-3]	+5 GND	J3
W5	[1-2]* [2-3]	+5 GND	J4

* = default

82C55A OUTPUT DRIVE CAPABILITIES

When a line is configured as an output, it can sink a maximum of 2.5 mA at +0.4V and can source a minimum of 2.5 mA at +2.4V. When driving opto modules, the output can sink 15 mA at 1.0V.

DRIVING OPTO RACKS

The 5600 can drive up to four MPB–8, –16 or –24 series opto mounting racks via a CMA–26 cable interface. Use isolator modules when driving or receiving signals from high voltage and/or high current devices. Opto–isolation also eliminates ground loops and significantly reduces the chance that noise will invade the system.

To drive opto module racks, plug one end of a CMA–26 cable into one of the J connectors that you want to use and the other end into the MPB opto mounting rack. Run ground and +5V to the mounting rack.

Use Opto Channel table to determine the corresponding opto channel for a particular 82C55A port. Remember to add the base address of the card. For example, suppose the base address is 110H, the following would be entered into the program:

```
A=INP(&H119)
```
reads opto rack on J3, channels 16–23

Opto Channels					
Channel	**82C55 Port**	**J1 Addr**	**J2 Addr**	**J3 Addr**	**J4 Addr**
0-3	Lower C	2	6	0AH	0EH
4-7	Upper C	2	6	0AH	0EH
8-15	A	0	4	08H	0CH
16-23	B	1	5	09H	0DH

TROUBLESHOOTING

If you have difficulty getting your system to work properly, remove all expansion cards except the 5600 Digital I/O Card from your system and check the power module and jumper configurations.

Power Module

The power module voltage should be 5V ±0.25V when measured at the connector pins. The power module ripple should be less than 50 mV.

Jumper Configuration

The 5600 is shipped with jumper connections in place for Base I/O Address 100H. Jumper changes are usually not needed to get the system running. If you changed the jumpers and the system is not working properly, return the system to the original jumper positions. If you still encounter difficulties, please contact Technical Support.

TECHNICAL ASSISTANCE

Carefully recheck your system before calling Technical Support. Run as many tests as possible; the more information you can provide, the easier it will be for the Technical Support staff to help you solve the problem. For technical assistance, please call 303–426–4521.

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TECHNICAL SPECIFICATIONS

The 5600 accepts switch closures and logic inputs; drives displays and LEDs; and interfaces with opto mounting racks. Each I/O line has a 10K pullup resistor; external resistors are not required when using switch contacts. The 5600 will interface with most parallel ports, including LCD and DP (vacuum fluorescent) series displays, printers, and single LEDs. The I/O levels are 0–5 volts and are compatible with logic levels.

Mapping

Occupies 16 I/O port addresses—ports 100H–10FH as shipped. May be remapped by jumper to any of eight consecutive I/O port addresses on 16 byte boundaries.

DC Characteristics

Input Low: –0.3V to +0.8V.
Input High: 2V to Vcc.
Output Low: 0.45V maximum.
Output High: 2.4V minimum.

Connectors

Four male 26–position, straight I/O connectors (Ansley #609–1007). Mates with Octagon CMA–26 cable.

Opto Rack Interface

Directly drives Octagon MPB series opto racks using CMA–26 cable.

Software Support

The 5600 is supported by Octagon's CAMBASIC IV software.

Bus Compatibility

Electrically compatible with the PC bus; designed to be used in the Micro PC card cage with Octagon's Micro PC Control Cards. May

be used with AT–sized PC's if used in conjunction with adapter bracket.

Power Requirements

VCC = 5V ± 0.25V at 35 mA typical, 75 mA maximum.

Environmental

Operating Temperature:	–40° to 85° C
Operating Humidity:	5 to 95% RH, noncondensing.

Size

4.5 in. x 4.9 in. Requires one Micro PC card cage slot.

JUMPER CONFIGURATIONS

W1: Base Address Select

Pins Jumpered	Base Address
[1–2], [3–4], [5–6]	100H*
[3–4], [5–6]	110H
[1–2], [5–6]	120H
[5–6]	130H
[1–2], [3–4]	140H
[3–4]	150H
[1–2]	160H
Not Jumpered	170H

* = default

CONNECTOR PINOUTS

J1–J4: Connector Pinouts

Pin #	Function
19	Port A, line 0
21	Port A, line 1
23	Port A, line 2
25	Port A, line 3
24	Port A, line 4
22	Port A, line 5
20	Port A, line 6
18	Port A, line 7
10	Port B, line 0
8	Port B, line 1
4	Port B, line 2
6	Port B, line 3
1	Port B, line 4
3	Port B, line 5
5	Port B, line 6
7	Port B, line 7
13	Port C, line 0
16	Port C, line 1
15	Port C, line 2
17	Port C, line 3
14	Port C, line 4
11	Port C, line 5
12	Port C, line 6
9	Port C, line 7
2	+5V
26	Common

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INTEL 82C55A DATA SHEET

The material in this appendix is Copyright 1992, Intel Corporation.

intel.

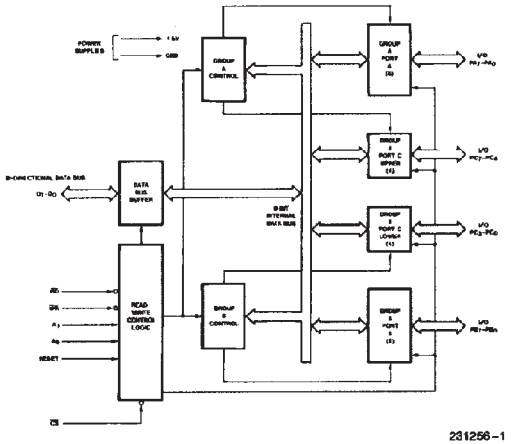
82C55A
CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- **Compatible with all Intel and Most Other Microprocessors**
- **High Speed, "Zero Wait State" Operation with 5 MHz 8086/88 and 80186/188**
- **24 Programmable I/O Pins**
- **Low Power CHMOS**
- **Completely TTL Compatible**
- **Control Word Read-Back Capability**
- **Direct Bit Set/Reset Capability**
- **2.5 mA DC Drive Capability on all I/O Port Outputs**
- **Available in 40-Pin DIP and 44-Pin PLCC**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

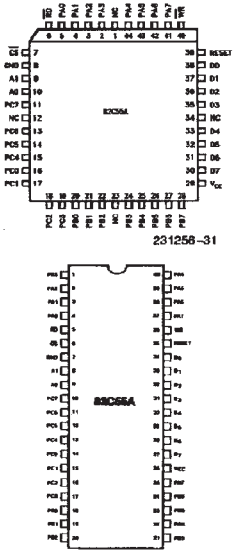
In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.



231256-1

Figure 1. 82C55A Block Diagram



231256-31

231256-2

Figure 2. 82C55A Pinout
Diagrams are for pin reference only. Package sizes are not to scale.

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Order Number: 231256-004

Table 1. Pin Description

Symbol	Pin Number Dip	Pin Number PLCC	Type	Name and Function
PA_{3-0}	1–4	2–5	I/O	**PORT A, PINS 0–3:** Lower nibble of an 8-bit data output latch/ buffer and an 8-bit data input latch.
$\overline{RD}$	5	6	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	6	7	I	**CHIP SELECT:** A low on this input enables the 82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
GND	7	8		**System Ground**
A_{1-0}	8–9	9–10	I	**ADDRESS:** These input signals, in conjunction $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the control word registers.

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control
					Disable Function
X	X	X	X	1	Data Bus - 3 - State
X	X	1	1	0	Data Bus - 3 - State

PC_{7-4}	10–13	11,13–15	I/O	**PORT C, PINS 4–7:** Upper nibble of an 8-bit data output latch/ buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
PC_{0-3}	14–17	16–19	I/O	**PORT C, PINS 0–3:** Lower nibble of Port C.
PB_{0-7}	18–25	20–22, 24–28	I/O	**PORT B, PINS 0–7:** An 8-bit data output latch/buffer and an 8-bit data input buffer.
V_{CC}	26	29		**SYSTEM POWER:** + 5V Power Supply.
D_{7-0}	27–34	30–33, 35–38	I/O	**DATA BUS:** Bi-directional, tri-state data bus lines, connected to system data bus.
RESET	35	39	I	**RESET:** A high on this input clears the control register and all ports are set to the input mode.
$\overline{WR}$	36	40	I	**WRITE CONTROL:** This input is low during CPU write operations.
PA_{7-4}	37–40	41–44	I/O	**PORT A, PINS 4–7:** Upper nibble of an 8-bit data output latch/ buffer and an 8-bit data input latch.
NC		1, 12, 23, 34		No Connect

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82C55A FUNCTIONAL DESCRIPTION

General

The 82C55A is a programmable peripheral interface device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 82C55A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7–C4)
Control Group B - Port B and Port C lower (C3–C0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions. Figure 6 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A. One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both "pull-up" and "pull-down" bus hold devices are present on Port A.

Port B. One 8-bit data input/output latch/buffer. Only "pull-up" bus hold devices are present on Port B.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only "pull-up" bus hold devices are present on Port C.

See Figure 4 for the bus-hold circuit configuration for Port A, B, and C.

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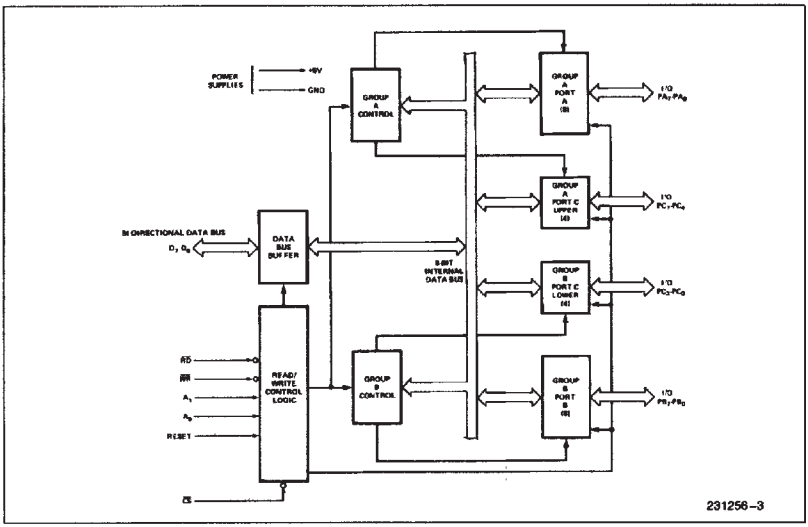
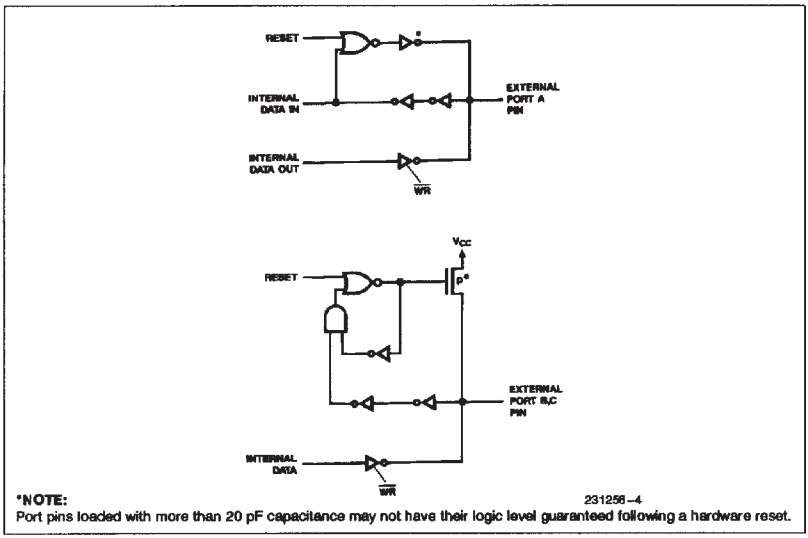


Figure 3. 82C55A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions



*NOTE:
Port pins loaded with more than 20 pF capacitance may not have their logic level guaranteed following a hardware reset.

Figure 4. Port A, B, C, Bus-hold Configuration

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82C55A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic input/output
Mode 1 — Strobed Input/output
Mode 2 — Bi-directional Bus

When the reset input goes "high" all ports will be set to the input mode with all 24 port lines held at a logic "one" level by the internal bus hold devices (see Figure 4 Note). After the reset is removed the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown devices in "all CMOS" designs. During the execution of the system program, any of the other modes may be selected by using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

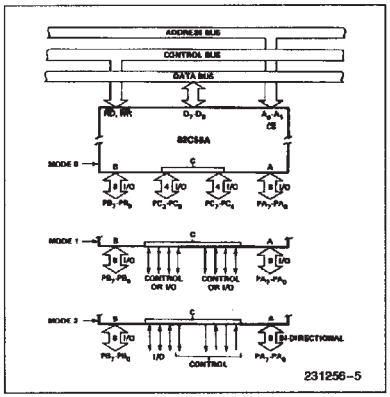

Figure 5. Basic Mode Definitions and Bus Interface

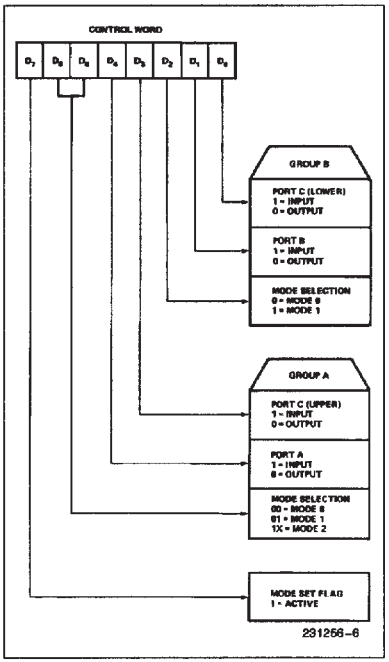

Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

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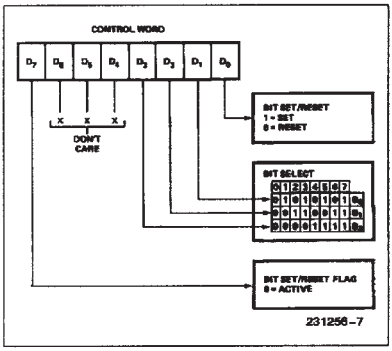

Figure 7. Bit Set/Reset Format

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is SET—Interrupt enable
(BIT-RESET)—INTE is RESET—Interrupt disable

Note:
All Mask flip-flops are automatically reset during mode selection and device Reset.

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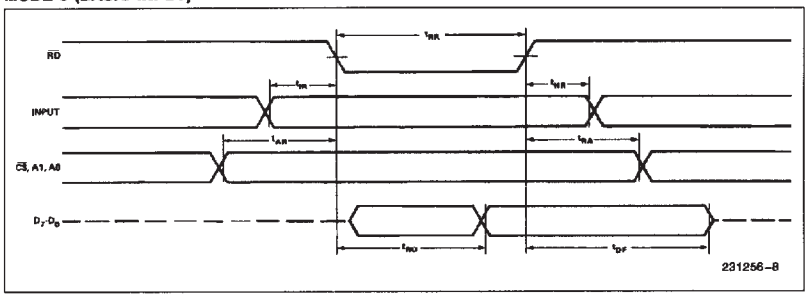
Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

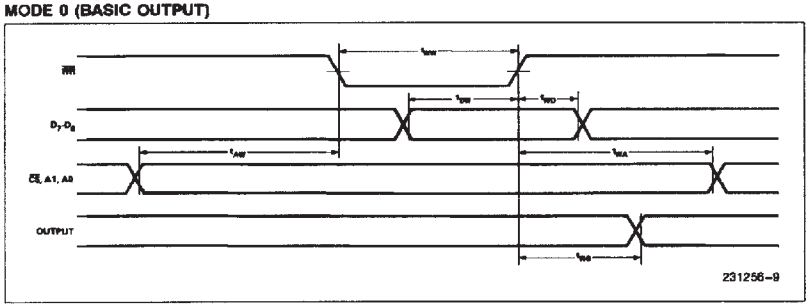
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)



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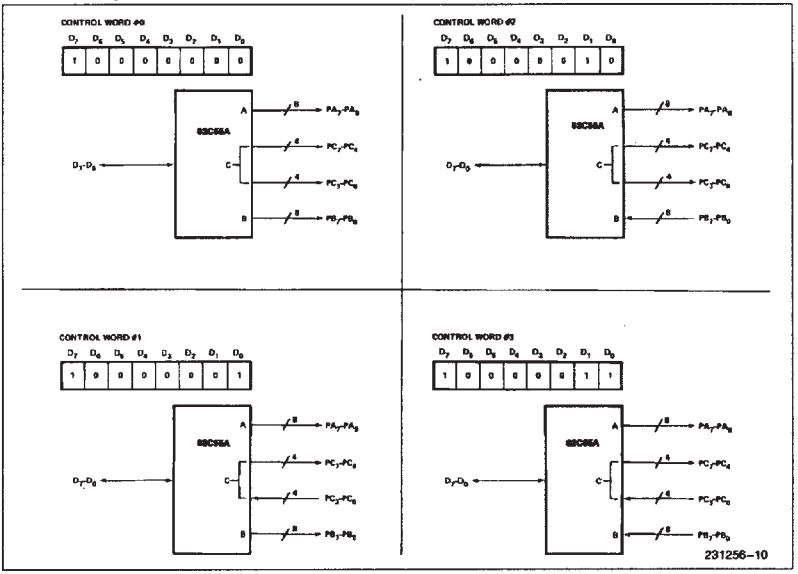
MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations



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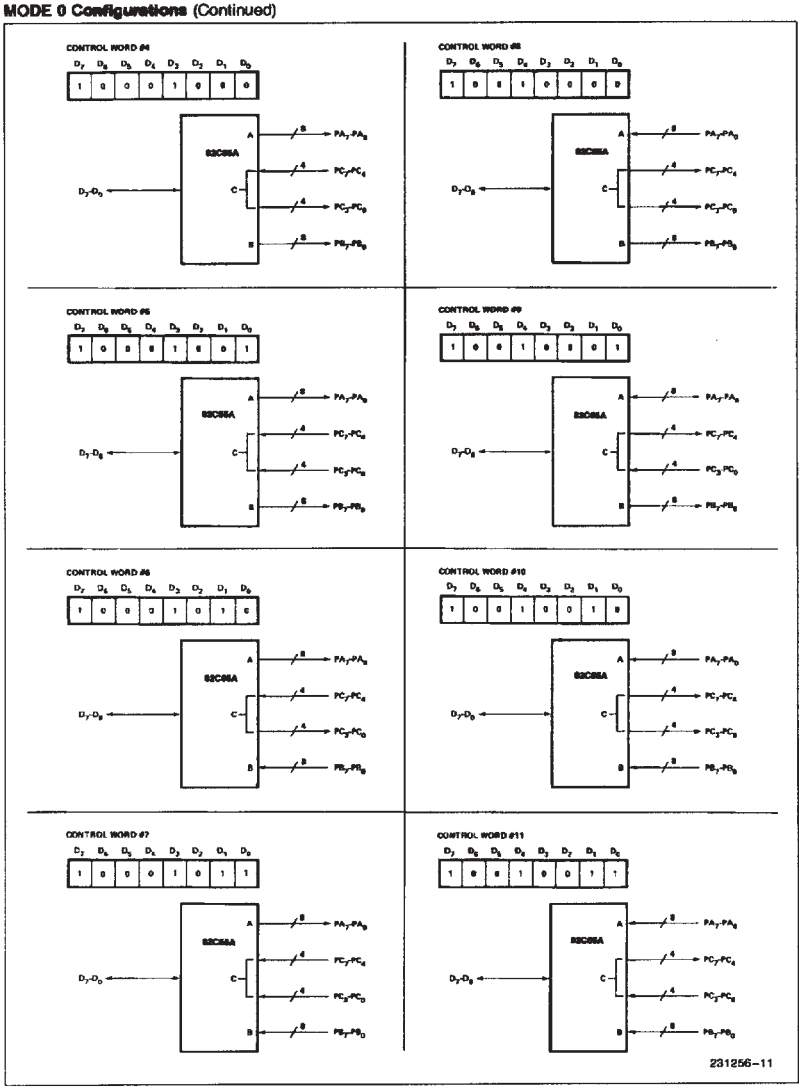
MODE 0 Configurations (Continued)



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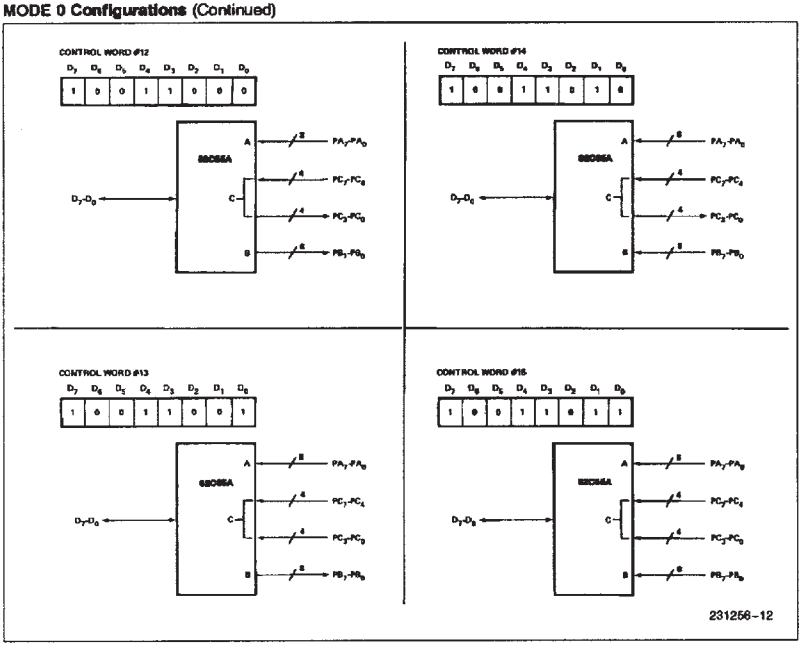
MODE 0 Configurations (Continued)



Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

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Input Control Signal Definition

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

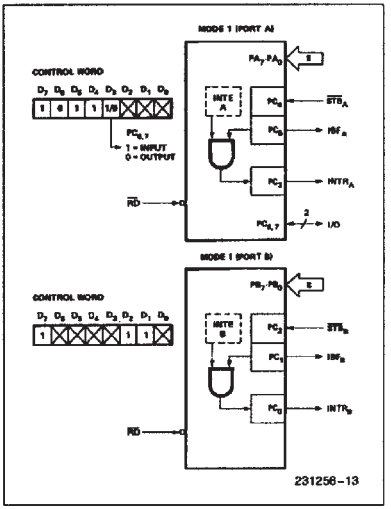

Figure 8. MODE 1 Input

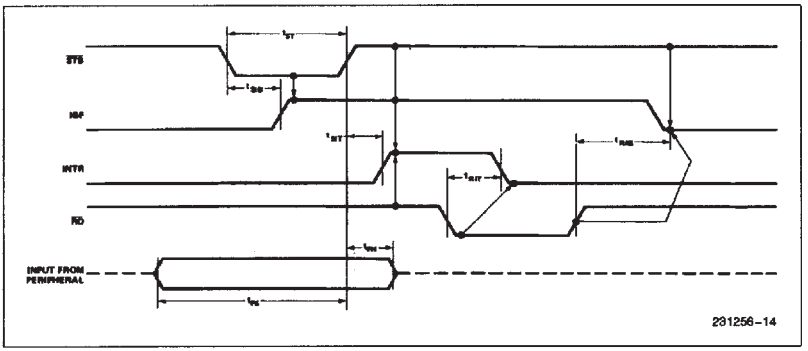

Figure 9. MODE 1 (Strobed Input)

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Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 82C55A that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

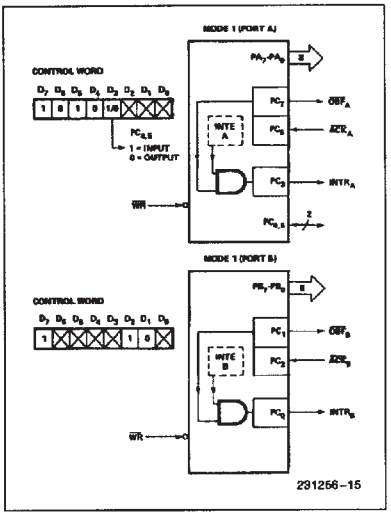

Figure 10. MODE 1 Output

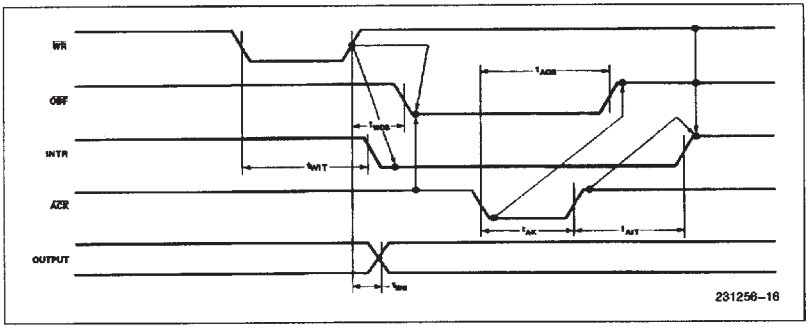

Figure 11. MODE 1 (Strobed Output)

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Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

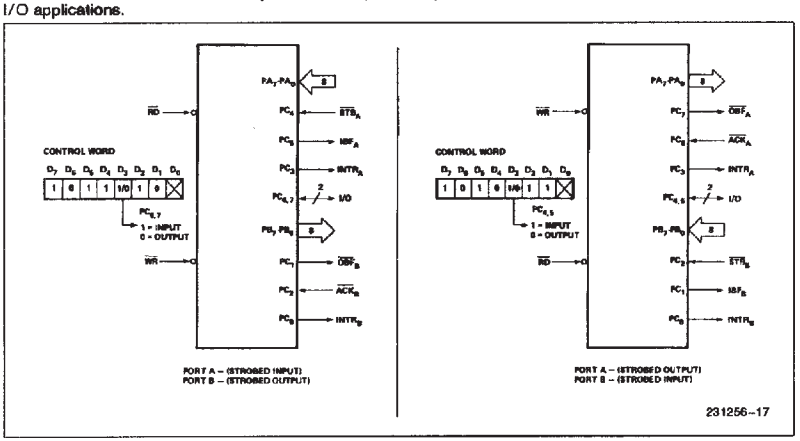

Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A **only.**
- One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

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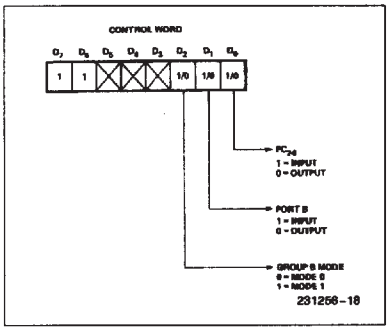

Figure 13. MODE Control Word

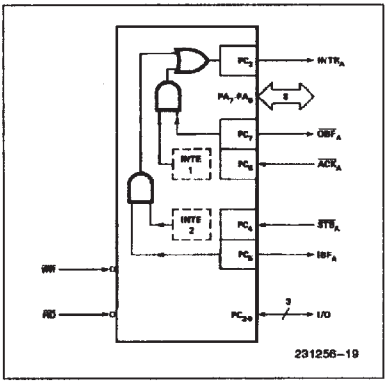

Figure 14. MODE 2

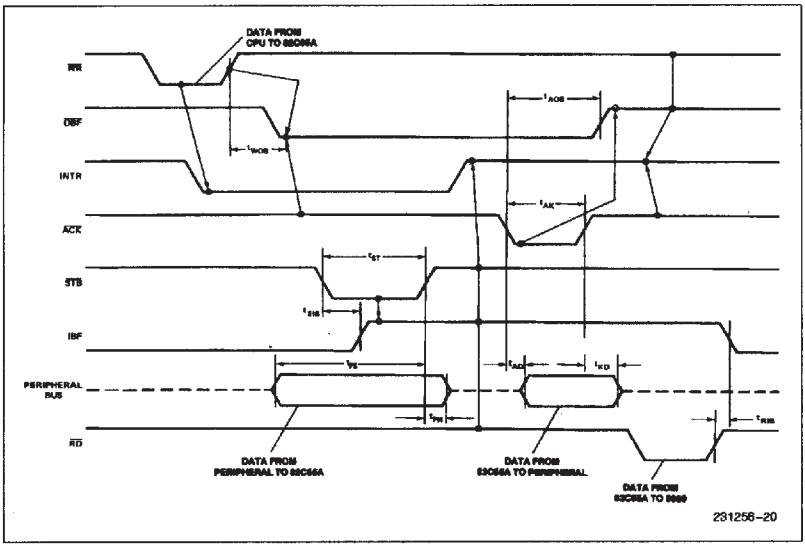

Figure 15. MODE 2 (Bidirectional)

NOTE:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and STB occurs before $\overline{RD}$ is permissible.
(INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

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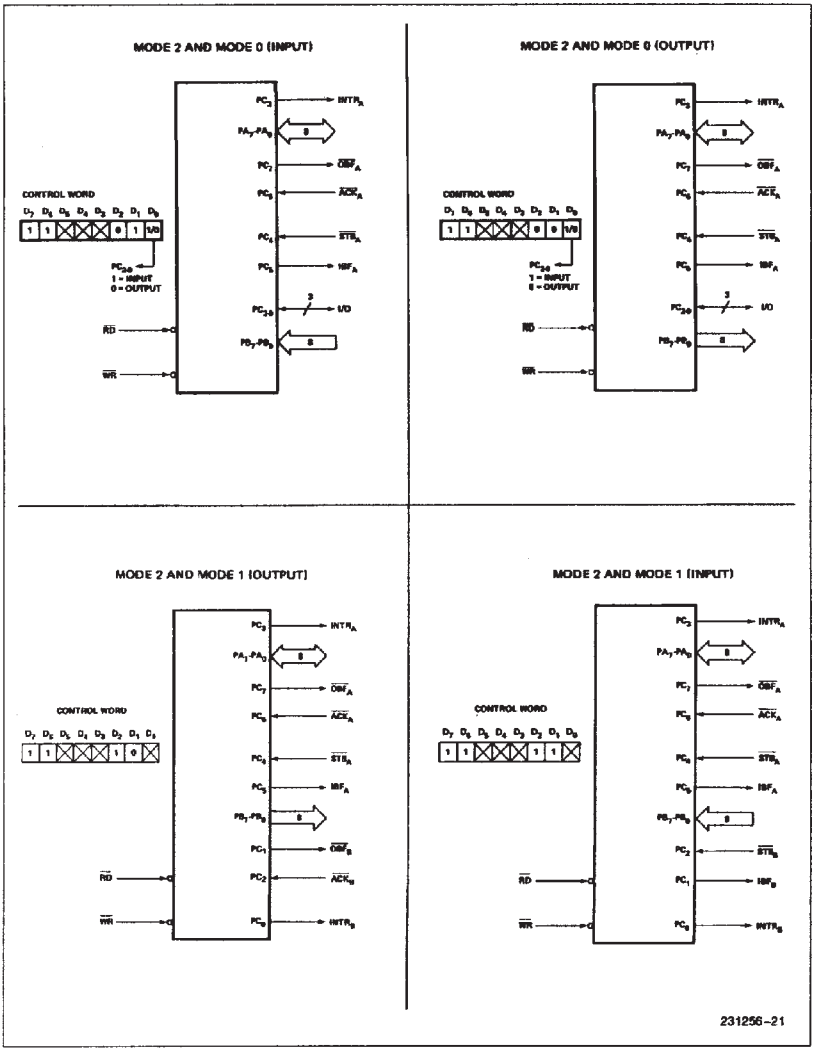

Figure 16. MODE ¼ Combinations

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Mode Definition Summary

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA_0	IN	OUT	IN	OUT	⟷
PA_1	IN	OUT	IN	OUT	⟷
PA_2	IN	OUT	IN	OUT	⟷
PA_3	IN	OUT	IN	OUT	⟷
PA_4	IN	OUT	IN	OUT	⟷
PA_5	IN	OUT	IN	OUT	⟷
PA_6	IN	OUT	IN	OUT	⟷
PA_7	IN	OUT	IN	OUT	⟷
PB_0	IN	OUT	IN	OUT	—
PB_1	IN	OUT	IN	OUT	—
PB_2	IN	OUT	IN	OUT	—
PB_3	IN	OUT	IN	OUT	—
PB_4	IN	OUT	IN	OUT	—
PB_5	IN	OUT	IN	OUT	—
PB_6	IN	OUT	IN	OUT	—
PB_7	IN	OUT	IN	OUT	—
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

MODE 0 OR MODE 1 ONLY

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 18.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 18.

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5 mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

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Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

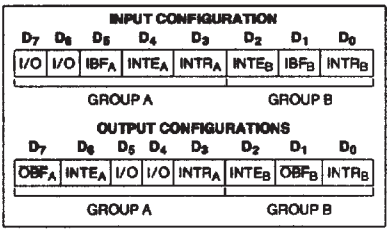
INPUT CONFIGURATION
D7 D6 D5 D4 D3 D2 D1 D0
I/O I/O IBFA INTEA INTRA INTEB IBFB INTRB
GROUP A
GROUP B
OUTPUT CONFIGURATIONS
D7 D6 D5 D4 D3 D2 D1 D0
OBFA INTEA I/O I/O INTRA INTEB OBFB INTRB
GROUP A
GROUP B

Figure 17a. MODE 1 Status Word Format

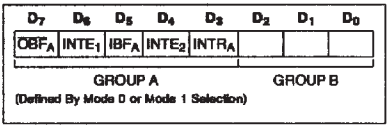

Figure 17b. MODE 2 Status Word Format

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
INTE A2	PC4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2

Figure 18. Interrupt Enable Flags in Modes 1 and 2

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias....0°C to + 70°C
Storage Temperature .....– 65°C to + 150°C
Supply Voltage .....– 0.5 to + 8.0V
Operating Voltage .....+ 4V to + 7V
Voltage on any Input.....GND – 2V to + 6.5V
Voltage on any Output ..GND – 0.5V to V_{CC} + 0.5V
Power Dissipation .....1 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, GND = 0V (T_A = –40°C to +85°C for Extended Temperture)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	3.0 V_{CC} – 0.4		V V	I_{OH} = –2.5 mA I_{OH} = –100 µA
I_{IL}	Input Leakage Current		±1	µA	V_{IN} = V_{CC} to 0V (Note 1)
I_{OFL}	Output Float Leakage Current		±10	µA	V_{IN} = V_{CC} to 0V (Note 2)
I_{DAR}	Darlington Drive Current	±2.5	(Note 4)	mA	Ports A, B, C R_{ext} = 500Ω V_{ext} = 1.7V
I_{PHL}	Port Hold Low Leakage Current	+50	+300	µA	V_{OUT} = 1.0V Port A only
I_{PHH}	Port Hold High Leakage Current	–50	–300	µA	V_{OUT} = 3.0V Ports A, B, C
I_{PHLO}	Port Hold Low Overdrive Current	–350		µA	V_{OUT} = 0.8V
I_{PHHO}	Port Hold High Overdrive Current	+350		µA	V_{OUT} = 3.0V
I_{CC}	V_{CC} Supply Current		10	mA	(Note 3)
I_{CCSB}	V_{CC} Supply Current-Standby		10	µA	V_{CC} = 5.5V V_{IN} = V_{CC} or GND Port Conditions If I/P = Open/High O/P = Open Only With Data Bus = High/Low $\overline{CS}$ = High Reset = Low Pure Inputs = Low/High

NOTES:
1. Pins A_1, A_0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Reset.
2. Data Bus; Ports B, C.
3. Outputs open.
4. Limit output current to 4.0 mA.

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CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	Unmeasured pins returned to GND f_c = 1 MHz(5)
$C_{I/O}$	I/O Capacitance		20	pF	

NOTE:
5. Sampled not 100% tested.

A.C. CHARACTERISTICS

T_A = 0° to 70°C, V_{CC} = +5V ±10%, GND = 0V

T_A = −40°C to +85°C for Extended Temperature

BUS PARAMETERS

READ CYCLE

Symbol	Parameter	82C55A-2		Units	Test Conditions
		Min	Max		
t_{AR}	Address Stable Before $\overline{RD}\downarrow$	0		ns	
t_{RA}	Address Hold Time After $\overline{RD}\uparrow$	0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	150		ns	
t_{RD}	Data Delay from $\overline{RD}\downarrow$		120	ns	
t_{DF}	$\overline{RD}\uparrow$ to Data Floating	10	75	ns	
t_{RV}	Recovery Time between $\overline{RD}/\overline{WR}$	200		ns	

WRITE CYCLE

Symbol	Parameter	82C55A-2		Units	Test Conditions
		Min	Max		
t_{AW}	Address Stable Before $\overline{WR}\downarrow$	0		ns	
t_{WA}	Address Hold Time After $\overline{WR}\uparrow$	20		ns	Ports A & B
		20		ns	Port C
t_{WW}	$\overline{WR}$ Pulse Width	100		ns	
t_{DW}	Data Setup Time Before $\overline{WR}\uparrow$	100		ns	
t_{WD}	Data Hold Time After $\overline{WR}\uparrow$	30		ns	Ports A & B
		30		ns	Port C

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OTHER TIMINGS

Symbol	Parameter	82C55A-2		Units Conditions	Test
		Min	Max		
t_{WB}	$\overline{WR}$ = 1 to Output		350	ns	
t_{IR}	Peripheral Data Before $\overline{RD}$	0		ns	
t_{HR}	Peripheral Data After $\overline{RD}$	0		ns	
t_{AK}	$\overline{ACK}$ Pulse Width	200		ns	
t_{ST}	$\overline{STB}$ Pulse Width	100		ns	
t_{PS}	Per. Data Before $\overline{STB}$ High	20		ns	
t_{PH}	Per. Data After $\overline{STB}$ High	50		ns	
t_{AD}	$\overline{ACK}$ = 0 to Output		175	ns	
t_{KD}	$\overline{ACK}$ = 1 to Output Float	20	250	ns	
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0		150	ns	
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1		150	ns	
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1		150	ns	
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0		150	ns	
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0		200	ns	
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1		150	ns	
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1		150	ns	
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0		200	ns	see note 1
t_{RES}	Reset Pulse Width	500		ns	see note 2

NOTE:
1. INTR ↑ may occur as early as $\overline{WR}$ ↓.
2. Pulse width of initial Reset pulse after power on must be at least 50 µSec. Subsequent Reset pulses may be 500 ns minimum.

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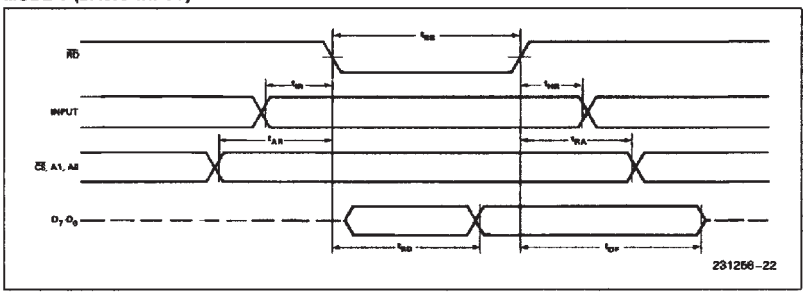
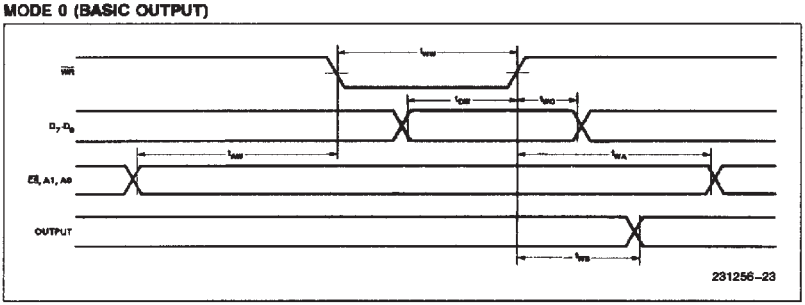
WAVEFORMS

MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)



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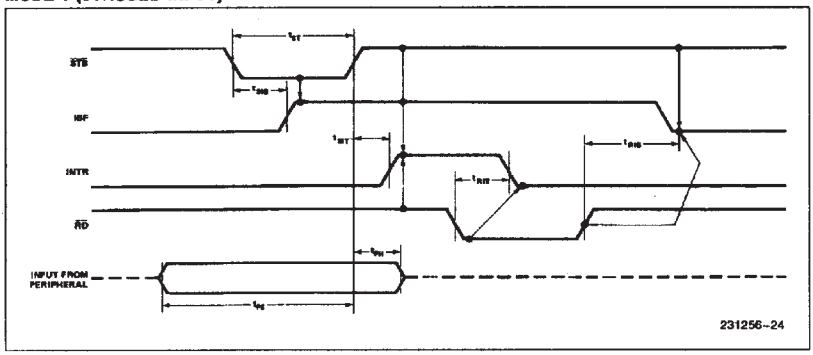
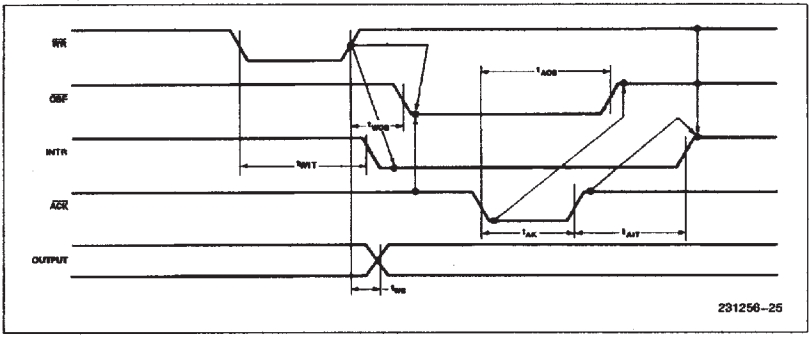
WAVEFORMS (Continued)

MODE 1 (STROBED INPUT)



MODE 1 (STROBED OUTPUT)



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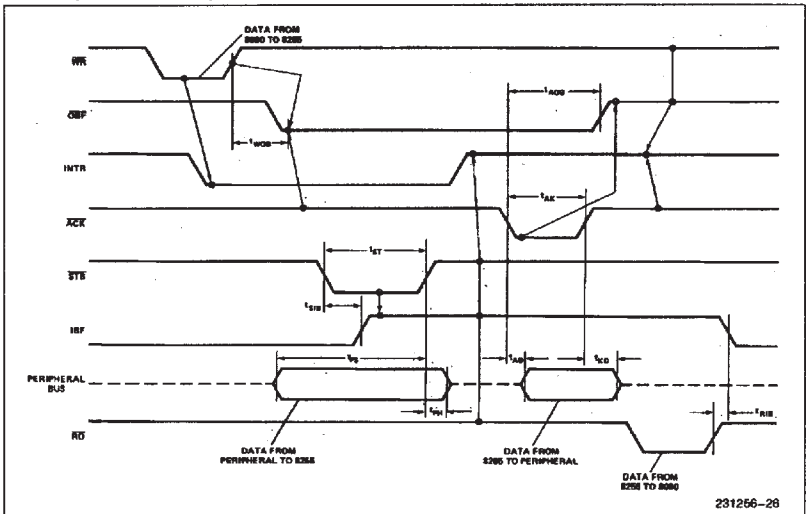
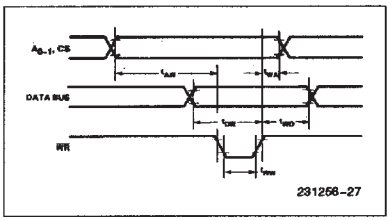
WAVEFORMS (Continued)

MODE 2 (BIDIRECTIONAL)

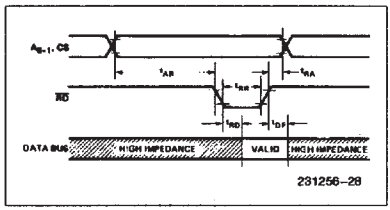


Note:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ AND $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

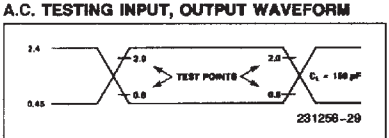
WRITE TIMING



READ TIMING

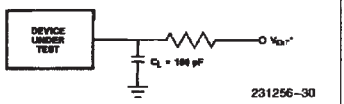


A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing Inputs Are Driven At 2.4V For A Logic 1 And 0.45V For A Logic 0 Timing Measurements Are Made At 2.0V For A Logic 1 And 0.8 For A Logic 0.

A.C. TESTING LOAD CIRCUIT



*V_{EXT} Is Set At Various Voltages During Testing To Guarantee The Specification. C_L Includes Jig Capacitance.

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2. Products which have been subject to power supply reversal, misuse, neglect, accident, or improper installation.
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1. Octagon's goal is to ship your product within 10 working days of receipt.
2. If a product should fail during the warranty period, it will be repaired free of charge. For out of warranty repairs, the customer will be invoiced for repair charges at current standard labor and materials rates.
3. Customers that return products for repairs, within the warranty period, and the product is found to be free of defect, may be liable for the minimum current repair charge.

RETURNING A PRODUCT FOR REPAIR

Upon determining that repair services are required, the customer must:

1. Obtain an RMA (Return Material Authorization) number from the Customer Service Department, 303-430–1500.
2. If the request is for an out of warranty repair, a purchase order number or other acceptable information must be supplied by the customer.
3. Include a list of problems encountered along with your name, address, telephone, and RMA number.
4. Carefully package the product in an antistatic bag. (Failure to package in antistatic material will VOID all warranties.) Then package in a safe container for shipping.
5. Write RMA number on the outside of the box.
6. For products under warranty, the customer pays for shipping to Octagon. Octagon pays for shipping back to customer.
7. Other conditions and limitations may apply to international shipments.

NOTE: PRODUCTS RETURNED TO OCTAGON FREIGHT COLLECT OR WITHOUT AN RMA NUMBER CANNOT BE ACCEPTED AND WILL BE RETURNED FREIGHT COLLECT.

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There will be a 15% restocking charge on returned product that is unopened and unused, if Octagon accepts such a return. Returns will not be accepted 30 days after purchase. Opened and/or used products, non-standard products, software and printed materials are not returnable without prior written agreement.

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